WHAT IS CLAIMED IS:

1. A method of writing information to a magnetic memory device, the magnetic memory device including a plurality of wordlines in a first wiring level positioned in a first direction, a plurality of bitlines in a second wiring level positioned in a second direction, and a plurality of magnetic memory cells, each magnetic memory cell being proximate an intersection of a wordline and a bitline, the magnetic memory device having a write path, the method comprising:

precharging the write path of the magnetic memory device;

after precharging, then selecting at least one magnetic memory cell; and

writing to the at least one magnetic memory cell.

2. The method according to Claim 1, wherein precharging the write path comprises precharging at least one of the wordlines to a first write voltage.

3. The method according to Claim 2, wherein precharging at least one of the wordlines comprises precharging all of the wordlines to the first write voltage.

4. The method according to Claim 2, wherein precharging the write path comprises precharging at least one of the bitlines to a second write voltage before selecting the at least one magnetic memory cell.

5. The method according to Claim 4, wherein precharging at least one of the bitlines comprises precharging all of the bitlines to the second write voltage.

6. The method according to Claim 3, wherein the magnetic memory cells are arranged in a plurality of sub-arrays, wherein a local write current generator is coupled to each sub-array, and a global reference current generator is coupled to each local write current generator, further comprising:

sending a global reference current from the global reference current generator to each local write current generator;

flowing the first write current from a local write current generator to the at least one magnetic memory cell; and

flowing the second write current from the local write current generator to the at least one magnetic memory cell.

7. The method according to Claim 6, further comprising precharging the inputs to the local write current generator before selecting the at least one magnetic memory cell.

8. The method according to Claim 6, further comprising coupling a fast on circuit between the sub-arrays and the local write current generator or between the global reference current generator and the local write current generators.

9. The method according to Claim 8, wherein coupling the fast on circuit comprises:

coupling a first transistor to a first reference voltage;

coupling a transfer gate to the first transistor;

coupling an enable input of a comparator to the transfer gate;

coupling a second transistor to an output of the comparator; and

coupling a third transistor to an input of the comparator and the transfer gate, wherein an input of the comparator and the second transistor are coupled to a second reference voltage of the sub-array or the local write current generator, wherein a start signal input to the fast on circuit triggers the precharging of the second reference voltage of the sub-array or the local write current generator.

10. The method according to Claim 6, wherein the global reference current generator comprises a precharge mode current reference generator and an active mode reference current generator, a control logic circuit coupled to the active mode reference current generator, the control logic circuit also being coupled to an oscillator, the oscillator being coupled to the precharge mode current reference generator, further comprising:

generating the global reference current from either the precharge mode current reference generator in a precharge mode or from the active mode reference current generator in an active mode.

11. The method according to Claim 10, further comprising sending a control signal to an input of the control logic circuit to select the precharge mode or the active mode.

12. The method according to Claim 10, wherein the oscillator periodically signals the precharge mode current reference generator to recharge a voltage potential for the global reference current in the precharge mode.

13. The method according to Claim 1, wherein writing to the at least one magnetic memory cell comprises:

first, applying a first current to a wordline of the at least one selected magnetic memory cell; then

second, applying a second current to a bitline of the at least one selected magnetic memory cell.

14. The method according to Claim 13, wherein writing to the at least one magnetic memory cell further comprises, after applying the second current to the bitline of the at least one selected magnetic memory cell:

third, removing the first current from the wordline of the at least one selected magnetic memory cell; then

fourth, removing the second current from the bitline of the at least one selected magnetic memory cell.

15. The method according to Claim 1, wherein the magnetic memory device comprises a magnetic random access memory (MRAM) device, and wherein the magnetic memory cells comprise magnetic tunnel junctions (MTJ's).

16. The method according to Claim 1, wherein the time required to precharge the write path is hidden in an address decoding time or in a redundancy evaluation time of the magnetic memory device.

17. A magnetic memory device, comprising:

a plurality of wordlines in a first wiring level positioned in a first direction;

a plurality of bitlines in a second wiring level positioned in a second direction;

a plurality of magnetic memory cells, each magnetic memory cell being proximate an intersection of a wordline and bitline, the magnetic memory cells being arranged in a plurality of sub-arrays;

a local write current generator coupled to each sub-array, the local write current generators having at least one input; and

a global reference current generator coupled to the at least one input of the local write current generators, wherein the global reference current generator precharges the at least one input of the local write current generators with a global reference current before at least one magnetic memory cell is written to in a write operation.

18. The magnetic memory device according to Claim 17, wherein the global reference current generator precharges the local write current generator input before the at least one magnetic memory cell is selected.

19. The magnetic memory device according to Claim 17, wherein the local write current generator precharges at least one of the wordlines with a first write voltage and precharges at least one of the bitlines with a second write voltage.

20. The magnetic memory device according to Claim 19, wherein the local write current generator precharges all of the wordlines to the first write voltage and precharges all of the bitlines to the second write voltage.

21. The magnetic memory device according to Claim 19, wherein the local write current generator sends a first write current to the at least one magnetic memory cell, and wherein the local write current generator sends a second write current to the at least one magnetic memory cell.

22. The magnetic memory device according to Claim 17, wherein the at least one magnetic memory cell is written to by first, applying a first current to a wordline of the at least one selected magnetic memory cell, then second, applying a second current to a bitline of the at least one selected magnetic memory cell.

23. The magnetic memory device according to Claim 22, wherein the at least one magnetic memory cell is written to by, after applying the second current to the bitline of the at least one selected magnetic memory cell, third, removing the first current from the wordline of the at least one selected magnetic memory cell, and then fourth, removing the second current from the bitline of the at least one selected magnetic memory cell.

24. The magnetic memory device according to Claim 17, wherein the magnetic memory device comprises a magnetic random access memory (MRAM) device, and wherein the magnetic memory cells comprise magnetic tunnel junctions (MTJ's).

25. The magnetic memory device according to Claim 17, wherein the time required to precharge the local write current generator inputs with a global reference current is hidden in an address decoding time or in a redundancy evaluation time of the magnetic memory device.

26. The magnetic memory device according to Claim 17, wherein the global reference current generator comprises:

a precharge mode current reference generator;

an active mode reference current generator;

a control logic circuit coupled to the active mode reference current generator; and

an oscillator coupled between the control logic circuit and the precharge mode current reference generator, wherein the global reference current is generated from either the precharge mode current reference generator in a precharge mode or from the active mode reference current generator in an active mode.

27. The magnetic memory device according to Claim 26, wherein a control signal sent to an input of the control logic circuit selects the precharge mode or the active mode.

28. The magnetic memory device according to Claim 26, wherein the oscillator periodically signals the precharge mode current reference generator to recharge a voltage potential for the global reference current.

29. The magnetic memory device according to Claim 17, further comprising a fast on circuit coupled between the sub-arrays and the local write current generator or between the local write current generator and the global reference current generator.

30. The magnetic memory device according to Claim 29, wherein the fast on circuit comprises:

a first transistor coupled to a first reference voltage;

a transfer gate coupled to the first transistor;

a comparator coupled to the transfer gate at an enable input of the comparator;

a second transistor coupled to an output of the comparator; and

a third transistor coupled to an input of the comparator and the transfer gate, wherein an input of the comparator and the second transistor are coupled to a second reference voltage of the sub-array or the local write current generator, wherein a start signal input to the fast on circuit triggers the precharging of the second reference voltage.

31. A global reference current generator for a magnetic memory device, comprising:

a precharge mode current reference generator;

an active mode reference current generator;

a control logic circuit coupled to the active mode reference current generator; and

an oscillator coupled between the control logic circuit and the precharge mode current reference generator, wherein a global reference current is generated from either the precharge mode current reference generator in a precharge mode or from the active mode reference current generator in an active mode.

32. The global reference current generator according to Claim 31, wherein a control signal sent to an input of the control logic circuit selects the precharge mode or the active mode.

33. The global reference current generator according to Claim 31, wherein the oscillator periodically signals the precharge mode current reference generator to recharge a voltage potential for the global reference current.

34. A circuit, comprising:

a first transistor coupled to a first reference voltage;

a transfer gate coupled to the first transistor;

a comparator coupled to the transfer gate at an enable input of the comparator;

a second transistor coupled to an output of the comparator; and

a third transistor coupled to an input of the comparator and the transfer gate, wherein an input of the comparator and the second transistor are coupled to a second reference voltage, wherein a start signal input to the transfer gate triggers the charging of the second reference voltage to a predetermined voltage level.

35. The circuit according to Claim 34, wherein the first transistor and the third transistor comprise PFET transistors, and wherein the second transistor comprises an NFET transistor.

36. The circuit according to Claim 34, wherein the first transistor and the third transistor comprise NFET transistors, and wherein the second transistor comprises a PFET transistor.